

86	N.C	--	(No Connection.)	Low	Low	Low	Low
87	N.C	--	(No Connection.)	Low	Low	Low	Low
88	N.C	--	(No Connection.)	Low	Low	Low	Low
89	FLD/T2 CLK	O	Serial clock output terminal for FIP driver and TEST_2(Factory use).	Not fix	Low	Low	Low
90	FLD/T2 DATA IN	I	Serial data input terminal for FIP driver and TEST_2(Factory use).	Not fix	In	In	In
91	FLD/T2 DATA OUT	O	Serial data output terminal for FIP driver and TEST_2(Factory use).	Not fix	Low	Low	Low
92	FLD_CS	O	Chip select terminal for FIP driver.	Not fix	Low	Low	Low
93	T.REEL.PULSE	I	Input terminal for Take-up Reel sensor pulse.	In	In	In	In
94	S.REEL.PULSE	I	Input terminal for Supply Reel sensor pulse.	In	In	In	In
95	DAVN	I	DAVN signal from Slicer	In	In	In	In
96	EEP_WR	O	Write enable for EEPROM H:READ only L:Write	High	High	Low	High
97	OSD IIC CLK	O	IIC clock for EEPROM,I/O and slicer	Not fix	Low	Low	Low
98	OSD IIC DATA	I/O	IIC data for EEPROM,I/O and slicer	Not fix	Low	Low	Low
99	MAIN IIC CLK	O	IIC clock for AV1CHIP,FM audio,Tuner,Decoder and RFC	Not fix	Low	Low	Low
100	MAIN IIC DATA	I/O	IIC data for AV1CHIP,FM audio,Tuner,Decoder and RFC	Not fix	Low	Low	Low
101	N.C	--	(No Connection.)	Low	Low	Low	Low
102	N.C	--	(No Connection.)	Low	Low	Low	Low
103	FG.AMP.OUT	O	Output from internal FG Amplifier	---	---	---	---
104	FG.AMP.IN	I	Input for internal FG Amplifier	---	---	---	---
105	GND(A)	I	GND	---	---	---	---
106	GND	I	GND	---	---	---	---
107	PFG	I	Cylinder PG/FG input terminal	---	---	---	---
108	OREF	O	Output from internal reference voltage (2.5V)	---	---	---	---
109	IREF	I	Input for internal reference voltage	---	---	---	---
110	to GND	I	Connect to GND	---	---	---	---
111	CTL.HEAD(-)	I	Input signal from CTL HEAD(+)	---	---	---	---
112	CTL.HEAD(+)	I	Input signal from CTL HEAD(-)	---	---	---	---
113	CTL.AMP.REF	I	Input for internal CTL amplifier reference voltage	---	---	---	---
114	PB.CTL.OUT	O	Output from internal CTL amplifier	---	---	---	---
115	+5V(A)	I	5V input terminal	---	---	---	---
116	+5V(AD)	I	5V input terminal	---	---	---	---